CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A multimedia data processing system, comprising:

a first integrated circuit, the first integrated circuit comprising:

a first logic block ~~generating a~~ receiving an encoded multimedia data stream;

a hardware encryption circuit coupled to the first logic block, the hardware encryption circuit encrypting the received data stream to generate an encrypted data stream with access control; and

a first Peripheral Component Interconnect Express (PCI-Express) - compatible interface circuit supporting data communication over a plurality of PCI-Express virtual channels, wherein the plurality of PCI-Express virtual channels comprises at least an unencrypted default virtual channel and a dedicated encrypted virtual channel, wherein the first PCI-Express-compatible interface circuit includes a first plurality of channel interconnects, each channel interconnect associated with a virtual channel among the plurality of virtual channels, wherein a first channel interconnect among the plurality of virtual channels is coupled to the hardware encryption circuit to

receive the encrypted data stream, and wherein the first PCI-Express-compatible interface circuit communicates the encrypted data stream from the hardware encryption circuit over the dedicated encrypted virtual channel;

a second integrated circuit coupled to the first integrated circuit by a PCI-Express-compatible interconnect, the second integrated circuit comprising:

a second PCI-Express-compatible interface circuit coupled to the PCI-Express-compatible interconnect to receive the encrypted data stream over the dedicated encrypted virtual channel, the second PCI-Express-compatible interface circuit comprising:

a second plurality of channel interconnects, each channel interconnect associated with a virtual channel among the plurality of virtual channels;

a hardware decryption circuit coupled to a first channel interconnect among the second plurality of channel interconnects for the second PCI-Express-compatible interface circuit and configured to decrypt the encrypted data stream; and

a second logic block coupled to the hardware decryption circuit ~~and configured to use~~ decoding the decrypted data stream, the decoding providing the multimedia stream to a subscriber authorized by the access control; and

control logic coupled to at least one of the first and second PCI-Express-compatible interface circuits and configured to communicate authorization data over the default virtual channel to authorize secure communication between the first and second integrated circuits over the dedicated encrypted virtual channel, wherein all data sent over the dedicated encrypted virtual channel are encrypted~~, and access control and decoding are separately performed on the first and second integrated circuits for the dedicated encrypted virtual channel~~.

2-3. (Canceled).

4. (Currently Amended) The ~~circuit arrangement of claim 2~~ system of claim 1, ~~further comprising:~~ wherein the first [[a]] logic block ~~coupled to the hardware encryption circuit and configured to output~~ outputs the multimedia data stream for communication over the ~~serial~~ PCI-Express-compatible interconnect to the hardware encryption circuit such that the multimedia data output by the logic block is encrypted prior to communication over the ~~serial~~ PCI-Express-compatible interconnect.

5. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, wherein the first logic block ~~is additionally configured to output~~ outputs additional data for

communication over ~~an~~ the unencrypted default virtual channel among the plurality of virtual channels.

6. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, wherein the logic block ~~is configured to output~~ outputs data over the ~~serial~~ PCI-Express-compatible interconnect solely over the dedicated encrypted virtual channel.

7. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, ~~further comprising:~~ wherein the [[a]] second logic block ~~coupled to the multi-channel serial interface circuit and configured to output~~ outputs data for communication over ~~an~~ the unencrypted default virtual channel among the plurality of virtual channels.

8. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, ~~further comprising:~~ wherein the [[a]] second logic block ~~coupled to the hardware encryption circuit and configured to output~~ outputs data for communication over the dedicated encrypted virtual channel.

9. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, ~~further comprising:~~ wherein the [[a]] hardware decryption circuit ~~coupled intermediate the multi channel serial interface circuit and the logic block, the hardware decryption~~

~~circuit configured to decrypt~~ decrypts encrypted data ~~received from the serial interconnect by the multi channel serial interface circuit and~~ communicated over the dedicated encrypted virtual channel.

10. (Currently Amended) The ~~circuit arrangement~~ system of claim 4, wherein the ~~plurality of virtual channels includes a~~ unencrypted default virtual channel ~~configured to communicate~~ communicates authorization data ~~for authorizing~~ to authorize secure communication over the dedicated encrypted virtual channel.

11-22. (Canceled)

23. (Currently Amended) A method of providing access control for a ~~digital~~ multimedia data stream, the method comprising:

demodulating an encoded multimedia signal to generate a first encrypted data stream;

decrypting the [[a]] first encrypted data stream in a first integrated circuit to generate a first decrypted data stream;

re-encrypting the first decrypted data stream in the first integrated circuit to generate a second encrypted data stream;

communicating the second encrypted data stream from the first integrated circuit to a second integrated circuit over a ~~multi-channel serial interconnect~~ PCI-Express-compatible interface to which the first and second integrated circuits are connected by communicating the second encrypted data stream over a dedicated encrypted virtual channel, among a plurality of virtual channels, the plurality of virtual channels comprising at least an unencrypted default virtual channel and a dedicated encrypted virtual channel, supported by ~~the multi-channel serial~~ a PCI-Express-compatible interconnect, wherein all data sent over the dedicated encrypted virtual channel are encrypted and wherein access control[[,]] and decoding are performed separately on the first and second integrated circuits for the dedicated encrypted virtual channel; ~~and~~

decrypting the second encrypted data stream in the second integrated circuit to generate a second decrypted data stream; and

decoding the second decrypted data stream to provide the multimedia signal to a subscriber authorized by the access control.

24-25. (Canceled).

26. (Currently Amended) The method of ~~claim 24~~ claim 23, further comprising:

performing MPEG decoding on the second decrypted data stream, wherein the ~~modulated input~~ multimedia signal comprises a satellite broadcast signal, and wherein the first encrypted data stream comprises an encrypted MPEG data stream.

27. (Previously Presented) The method of claim 23, further comprising:

performing regional access control on the first encrypted data stream.

28. (Previously Presented) The method of claim 23, further comprising:

performing subscriber access control on the first encrypted data stream.

29. (Previously Presented) The method of claim 23, further comprising:

disposing the first and second integrated circuits in a set top box.

30. (Previously Presented) The method of claim 23, further comprising:

disposing the first integrated circuit on an access card coupled to the second integrated circuit via a connector.

31. (Previously Presented) The method of claim 23, further comprising:

performing re-encryption of the first decrypted data stream with hardware encryption logic disposed on the first integrated circuit.

32. (Currently Amended) A ~~circuit arrangement~~ receiver circuit, comprising:

demodulation logic generating a first encrypted data stream from an encoded multimedia signal;

first decryption logic configured to perform access control, ~~and~~ to decrypt the [[a]] first encrypted data stream and to generate a first decrypted data stream, the first decryption logic disposed on a first integrated circuit in a processor chip set;

encryption logic configured to re-encrypt the first decrypted data stream and generate therefrom a second encrypted data stream;

second decryption logic decrypting the second encrypted data stream and generating a second decrypted data stream;

decoder logic on a second integrated circuit in the processor chip set, the decoder logic decoding the second decrypted data stream to provide the multimedia signal to a subscriber authorized by the access control; and

a ~~multi-channel serial~~ first PCI-Express-compatible interface circuit ~~configured to communicate~~ communicating the first and the second encrypted data stream over a ~~multi-channel serial~~ PCI-Express-compatible interconnect by communicating the second encrypted data stream over a dedicated encrypted

virtual channel, among a plurality of virtual channels, the plurality of virtual channels comprising at least an unencrypted default virtual channel and a dedicated encrypted virtual channel, supported by the multi-channel serial interconnect, wherein all data sent over the dedicated encrypted virtual channel are encrypted, ~~and~~ wherein access control[[,]] and decoding are performed separately on the first and second integrated circuits for the dedicated encrypted virtual channel.

33-35. (Canceled).

36. (Currently Amended) The ~~circuit arrangement of claim 35~~ receiver circuit of claim 32, wherein the ~~modulated input~~ encoded multimedia signal comprises a satellite broadcast signal, wherein the first encrypted data stream comprises an encrypted MPEG data stream, and wherein decoding the second decrypted data stream in the second integrated circuit comprises performing MPEG decoding on the second decrypted data stream.

37. (Currently Amended) The ~~circuit arrangement of claim 35~~ receiver circuit of claim 32, wherein the demodulation logic, the encryption logic, and the ~~multi-channel serial~~ first PCI-Express-compatible interface circuit are disposed on the first integrated circuit, wherein the second decryption logic is disposed on the

second integrated circuit, and wherein the second integrated circuit includes a second ~~multi-channel serial~~ PCI-Express-compatible interface circuit coupled to the ~~multi-channel serial~~ PCI-Express-compatible interconnect to receive the second encrypted data stream.

38. (Currently Amended) The ~~circuit arrangement of claim 32~~ receiver circuit of claim 32, wherein the first decryption logic performs regional access control on the first encrypted data stream.

39. (Currently Amended) The ~~circuit arrangement of claim 32~~ receiver circuit of claim 32, wherein the first decryption logic performs subscriber access control on the first encrypted data stream.

40-45. (Canceled)